13th International Workshop on Microprocessor Test and Verification Final Program
December 10-12, 2012
Hyatt Regency Hotel on Town Lake, Austin, Texas, USA
http://mtvcon.org

General Chair: Magdy Abadir (Freescale Semiconductor)
Program Co-Chair: Jay Bhadra (Freescale Semiconductor)
Program Co-Chair: Li-C. Wang (University of California at Santa Barbara)

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December 9, 2012

6-8pm: MTV Welcome Drink and Early Registration.
Location Hyatt Lobby Area Bar
Meet the MTV organizers to pick-up your registration material and network.

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Technical Program

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Day 1: December 10, 2012

7:30-8:00am: Registration and continental breakfast

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8:00-9:00 am: Plenary Session
Opening Remarks: Magdy Abadir, MTV General Chair (Freescale)

Keynote Address : Verification Complexity Challenges: Analytics to the Rescue
Speaker: Moshe Levinger (Manager, IBM Research Lab, Israel)

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9:00-10:00am: Session A. Formal Methods
Session Chair: Mark Nodine

A.1 Guaranteeing termination of fully symbolic timed forward model checking
Georges Morbé and Christoph Scholl (University of Freiburg, Germany)

A.2 Automatic Formal Correspondence Checking of ISA and RTL Microprocessor Description
Lukas Charvat, Ales Smrcka and Tomas Vojnar (Brno University of Technology, Czech Republic)

A.3 Assessing and Improving the Quality of Formal Verification Environments using Functional Qualification
Kai Yang, Luke Lin, Edward Chang, Tangent Wei, Michael Lyons and George Bakewell (SpringSoft Inc, USA/Taiwan, France)

10:00-10:15 am Coffee Break

10:15-11:15 am: Session B. Coherency Verification
Session Chair: John Dickol (Samsung)

B.1 Random Stimulus for Memory Coherency Verification of Heterogeneous System Architecture
Arthur Flatau, Russ Hunt, Minh Truong and Farhan Rahman (AMD, USA)

B.2 Verification of CGRA Executable Code and Debugging of Memory Dependence Violation
Heejun Shim, Minwook Ahn, Jinsae Jung, Yenjo Han and Soojung Ryu (Samsung Electronics, Korea)

B.3 Architectural Trace-Based Functional Coverage for Multiprocessor Verification
Biruk Mammo, Jim Larimer*, Dave Fan*, Matthew Morgan*, Eric Hennenhoefer* and Valeria Bertacco (University of Michigan, USA, *ARM, USA)

11:15-12:00 pm Session C. Special Session on Transactional Memories
Session Chair: Laurent Fournier (IBM)

C.1 Perspectives on Hardware Transactional Memory Design
Christopher J. Rossbach (Microsoft Research, USA)

C.2 Verification of Transactional Memory for the zEnterprise EC12 Processor
Brian W. Thompto (IBM, USA)

12:00-1:00 pm Lunch

1:00-1:30 pm Invited talk: Future of Heterogeneous Computing
Session Chair: Xiao (Sean) Sun (Freescale)

Speaker: David Shippy (Altera, USA)

1:30-2:30 pm PANEL: When Simulation suffices, who needs FPGA or Emulation?

Moderator: Sanjay Gupta (Freescale)

Participants:
Andrew Dauman (Synopsys)
Bill Neifert (Carbon)
Juergen Jaeger (Cadence)
Mike Pedneau (Jasper)
2:30-3:30pm: Session D. Low Power Verification and Test
Session Chair: Adam Abadir (AMD)

D.1 RTOS QoS for Power Management Tasks in Intel ATOM CPU
Aswin Ramachandran, Ed Welbon and Girish Jattani (Intel, USA)

D.2 New Process to Simultaneously Measure, Quantify, and Model Energy Efficient Performance
Markus Mattwandel (Intel, USA)

D.3 Deterministic ATPG for Low Capture Power Testing
Lung-Jen Lee (National Army Academy, Taiwan)

3:30-3:45pm Coffee Break

3:45-5:05pm: Session E. High Level Verification
Session Chair: Alan Hunter (ARM)

E.1 Novel Test Analysis to Improve Functional Verification Coverage - A Commercial Experiment
Wen Chen, Li-C. Wang, Jayanta Bhadra, Magdy S. Abadir, UCSB and Freescale.

E.2 Case study: Verification Framework of Samsung Reconfigurable Processor
Youngchul Cho, Seonghun Jeong, Jinsae Jung, Heejun Shim, Yenjo Han, Soojung Ryu and Jay Kim
(Samsung Advanced Institute of Technology, Korea)

E.3 On the reuse of RTL IPs for SysML model generation
Nicola Bombieri, Emad Samuel Malki Ebeid, Franco Fummi and Michele Lora (University of Verona,
Italy/Egypt)

E.4 Yes We Kanban!
Bryan Morris (Verilab, Canada)

6:30pm MTV Workshop Dinner

Venue: Fogo de Chão, 309 E. 3rd St., Austin, TX 78701, Phone: (512) 472-0220
A short (about 10 minutes) walk from Hyatt Fogo de Chão is located in downtown Austin. Fogo de
Chão is an authentic Brazilian steakhouse. http://www.fogodechao.com/locations/austin/

Transportation: Attendees can stroll to the restaurant.
Day 2: December 11, 2012

7:30-8:00am Registration and continental breakfast

8:00-8:40 am Invited talk: Test Plan Automation - the Next Leap in Test Generation Efficiency
Session Chair: Aseem Gupta (Freescale)
Speaker: Laurent Fournier (IBM Research, Haifa)

8:40-10:00am: Session F. Debug
Session Chair: Farhan Rahman (AMD)

F.1 Assertion Tailored to Fit a Test case
Jinsae Jung, Heejun Shim, Youngchul Cho, Yenjo Han and Soojung Ryu (Samsung Electronics, Korea)

F.2 Localization of Bugs in Processor Designs Using zamiaCAD Framework
Anton Tsepurov, Valentin Tihomirov, Maksim Jenihhin, Jaan Raik, Günter Bartsch**, Jorge Hernandez Meza Escobar* and Heinz-Dietrich Wuttke* (Tallinn University of Technology, Estonia, **zamiaCAD project founder, Germany, *Ilmenau University of Technology, Germany)

F.3 A Hybrid Approach for Fast and Accurate Trace Signal Selection for Post-Silicon Debug
Min Li and Azadeh Davoodi (University of Wisconsin – Madison, USA)

F.4 The Smartphone Approach to Making HVL Testbenches
Alex Melikian and Anders Nordstrom (Verilab, Canada)

10:00-10:15 am Coffee Break

10:15-11:15 am PANEL: My IP is fully verified. Will it work in SOC the first time?
Moderator: John Donovan (Editor/Publisher, Low-Power Publishing)

Participants:
Paul Graykowski (Synopsys)
John Goodenough (ARM)
Thomas L. Anderson (Breker Verification Systems, Inc)

11:15-12:00 pm Invited talk: Hardware Security Issues in a 3D-Die Stack: Implications for Test & Debug
Session Chair: Vivek Vedula (Freescale)
Speaker: Jennifer Dworak (Southern Methodist University, USA)

12:00-1:00 pm Lunch break
1:00-1:30 pm Invited talk: Use of Feed Forward Data to Effectively Reduce Test Escapes
Session Chair: Himyanshu Anand (Freescale)
Speaker: Keith Arnold (Optimal Test, USA)

1:30-2:45 pm PANEL: Can digital methods answer the mixed-signal verification and debug questions?
Moderator: Scott Little (Intel)
Participants:
Abhi Kolpekwar (Cadence)
Raul Camposano (Nimbic)
Tom Barrett (Intel)
Peng Li (Texas A&M)
Kai Yang (Springsoft)
Helene Thibieroz (Synopsys)

2:45-3:25 pm: Session G. SOC Verification
Session Chair: Neeta Ganguly (Intel)

G.1 IP to SoC Verification Reuse Methodology
Hassan Shehab, Matan Kacen and Kalita Dhrubajyoti (Intel, USA/Israel)

G.2 Pre-Si verification challenges of integrating third-party IPs
Sukumar Raghuram (Intel, USA)

3:25-3:40 pm Coffee Break

3:40-4:40 pm: Session H. Automatic Test Generation
Session Chair: Eric Hennenhoefer (ARM)

H.1 Random Test Program Generation for Reconfigurable Architectures
Seonghun Jeong, Youngchul Cho, Daeyong Shin*, Changyeon Jo*, Yenjo Han, Soojung Ryu, Jeongwook Kim and *Bernhard Egger (Samsung Advanced Institute of Technology, Korea, *Seoul National University, Korea)

H.2 Abstract-State Based X86 Random Stimulus Generation
Todd Dukes, Jason Yeh, Randall Metzger and Farhan Rahman (AMD, USA)

H.3 Automatic Generation of On-Line Test Programs through a Cooperation Scheme
Ernesto Sanchez, Lyl Ciganda, Marco Gaudesi, Giovanni Squillero, Evelyne Lutton* and Alberto Tonda** (Politecnico di Torino, Italy, *Université Paris-Sud, France, **Institut des Systèmes Complexes – Paris Île-de-France, France)
4:40-5:40 pm: Session J: BIST and Compression
Session Chair: Rajesh Raina (Freescale)

**J.1 Dual Linear Feedback Shift Register for Low Power BIST**
Lung-Jen Lee*, Wang-Dauh Tseng and Wen-Ting Yang (*National Army Academy, Taiwan, Yuan Ze University, Taiwan)

**J.2 Two-Way Multicasting for Test Data Compression**
Lung-Jen Lee*, Wang-Dauh Tseng and Wei-Shun Chen (*National Army Academy, Taiwan, Yuan Ze University, Taiwan)

**J.3 Selection of Optimum LFSR for BIST Architecture with Reduced Transition and Aliasing**
Afaq Ahmad (Sultan Qaboos University, Oman)

5:40pm Closing Remarks – Magdy Abadir (Freescale)
Day 3: December 12, 2012
Tutorials Day
(Free with MTV registration)
Venue: Freescale Semiconductor Inc.
7700 W Parmer Lane, Building A, Roundup Conference Room, Austin, TX 78729

8:00-9:15 am Tutorial: An introduction to practical implementation of Linear Feedback Shift Registers
Dr. Afaq Ahmad (Sultan Qaboos University, Oman)

9:15-9:30 am Break

9:30-10:45 am Tutorial: Getting started with Universal Verification Methodology (UVM)
Vanessa Cooper (Verilab, USA)

11:00 am-1:30 pm: DVClub Luncheon

DVClub Austin - Zihno Jusufovic - Processor Verification at AMD
Talk and Free lunch at the Cool River Cafe (4001 West Parmer Lane, Austin, Texas 78727)

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